What Is Claimed Is:

1. A self-test circuit that detects defects of a memory device, incorporated in the memory device having a memory control circuit that controls write and read operations with respect to a memory core in response to a command, comprising:

a test operation command generating circuit that, in self-test activated condition, generates a test operation command that designates said writing or reading, and that supplies the test operation command to said memory control circuit;

a test address generating circuit that, in said self-test activated condition, generates a test address and supplies the test address to said memory core;

a test data generating circuit that, in said self-test activated condition, generates test data and supplies the test data to said memory core; and

a test output circuit that compares read data from said memory core with said test data and stores information as to the result of this comparison, and outputs the information to the outside;

wherein said self-test circuit goes into the self-test activated condition in response to a self-test activation signal from outside.

2. The memory device self-test circuit of claim 1 further comprising a test operation mode selector circuit that,

in said self-test activated condition, generates a test operation mode signal that designates any of a plurality of test operation modes including said write and/or read,

wherein, in response to said test operation mode signal, said test operation command generating circuit generates said test operation command for executing said test operation mode.

3. The memory device self-test circuit of claim 2 wherein said test operation mode selector circuit generates said test operation mode signal by decoding a plurality of test operation mode input signals supplied from outside.

4. The memory device self-test circuit of claim 3 wherein said plurality of test operation mode input signals are serially input in synchronization with an input timing signal.

5. The memory device self-test circuit of claim 2 wherein said test operation mode selector circuit sequentially generates said plurality of test operation mode signals in said test activation condition.

6. The memory device self-test circuit of claim 1 wherein the self-test activation signal is one or other of a signal supplied from a self-test input terminal or a signal generated in response to a prescribed command of said memory

device.

7. The memory device self-test circuit of claim 6 wherein said self-test input terminal is maintained at a prescribed potential in the open condition.

8. The memory device self-test circuit of claim 1 wherein said test operation command generating circuit sequentially generates a plurality of test operation commands corresponding to operations including at least one of said write or read, every time a particular address is generated by said test address generating circuit.

9. The memory device self-test circuit of claim 1 wherein said test address generating circuit comprises an address counter and said test address is generated by counting an address timing signal for address incrementing or decrementing.

10. The memory device self-test circuit of claim 9 wherein said address counter of the test address generating circuit selectively outputs a non-inverted output or inverted output of the counter value, in accordance with said test operation mode signal.

11. The memory device self-test circuit of claim 1 wherein, when said test operation command corresponds to

write operation, said test data generating circuit supplies the test data to said memory core as write data and, when said test operation command corresponds to read operation, said test data generating circuit supplies the test data to said test output circuit as comparison data.

12. The memory device self-test circuit of claim 11 wherein said test data generating circuit generates said test data in a prescribed pattern in accordance with said test address signal in synchronization with said address timing signal.

13. The memory device self-test circuit of claim 1 wherein said test output circuit comprises a counter that counts the number of times of non-coincidence of said read data and the test data.

14. The memory device self-test circuit of claim 13 wherein the counter of said test output circuit has as its maximum count value a number of times of said non-coincidence corresponding to at least the maximum number of failed bits that can be rescued.

15. The memory device self-test circuit of claim 14 wherein the counter of said test output circuit generates an overflow signal when its count value exceeds said maximum count value, and outputs the fact that the overflow has

occurred.

16. The memory device self-test circuit of claim 1 wherein said test output circuit comprises a parallel/serial conversion circuit and serially outputs said comparison result information in synchronization with an output timing signal.

17. The memory device self-test circuit of claim 1 wherein said test output circuit outputs, as said comparison result information, information as to whether or not the number of times of non-coincidence of said read data and test data is equal to or below the number of times that can be rescued.

18. The memory device self-test circuit of claim 17 wherein said test output circuit further outputs, as said comparison result information, information that non-coincidence of said read data and test data did not occur.

19. The memory device self-test circuit of claim 17 wherein said test output circuit further outputs, as said comparison result information, the number of times of said non-coincidence.

20. The memory device self-test circuit of claim 4

wherein said input timing signal is a test clock signal that is generated based on a clock supplied from outside.

21. The memory device self-test circuit of claim 8 wherein said test operation command generating circuit generates said test operation command in synchronization with a command generation timing signal that is generated from a clock supplied from outside.

22. The memory device self-test circuit of claim 9 wherein said address timing signal is a test clock signal that is generated from a clock supplied from outside.

23. The memory device self-test circuit of claim 16 wherein said output timing signal is a test clock signal that is generated from a clock supplied from outside.

24. The memory device self-test circuit of claim 20, 21, 22 or 23 further comprising a clock multiplication circuit that generates an internally generated clock by multiplying said clock supplied from outside and

wherein said timing signal is generated from the internally generated clock.

25. The memory device self-test circuit of either of claim 21 or 22 further comprising an oscillator that generates an internally generated clock in the self-test

activated condition, and wherein said timing signal is generated from the internally generated clock.

26. A memory device including a memory core having a plurality of memory cells and a memory control circuit that controls write and read operations in respect of said memory core in response to an external command, in which writing or reading of said memory cells corresponding to an external address is performed, said memory device comprising:

a self-test circuit that detects defects of said memory device by assuming a self-test activated condition in response to a self-test activation signal from outside;

wherein said self-test circuit comprises:

a test operation command generating circuit that, in said test activated condition, generates a test operation command that designates said writing or reading and supplies the test operation command to said memory control circuit;

a test address generating circuit that, in said self-test activated condition, generates a test address and supplies the test address to said memory core;

a test data generating circuit that, in said self test activated condition, generates test data and supplies the test data as write data to said memory core; and

a test output circuit that compares the read data from said memory core with said test data and stores the comparison result information.

27. The memory device of claim 26 comprising:

a first selector that changes over said external command and said test command;

a second selector that changes over said external address and said test address; and

a third selector that changes over external write data supplied from outside and said test data.

28. The memory device of claim 27 further comprising:

a clock multiplier circuit that generates an internally generated clock by multiplying an external clock supplied from outside; and

a fourth selector that changes over said external clock and said internally generated clock.

29. The memory device of claim 27 further comprising:

an oscillator that generates an internally generated clock in the self-test activated condition; and

a fourth selector that changes over said external clock and said internally generated clock.

30. The memory device of claim 27 further comprising:

a data output circuit that outputs read data that is read from said memory cells; and

a fifth selector that changes over the comparison result information from said test output circuit and said read

data and supplies this to said data output circuit.

31. The memory device of claim 26, further comprising a self-test external terminal that is supplied with said self-test activation signal.

32. The memory device of claim 26 wherein said self-test activation signal is supplied by a prescribed external command.

33. The memory device of claim 27 wherein at least one of said first, second and third selectors is provided at a corresponding input circuit, and

said input circuit inputs an input signal that is changed over by said selector in synchronization with a first clock and said self-test circuit supplies to said selector a corresponding signal from among said test command, test address, or test data in synchronization with a second clock which is advanced in phase from said first clock.

34. The memory device of claim 33 wherein said input circuit comprises an input buffer that inputs an external command, external address, and/or external write data, and a latch circuit that latches the output of said input buffer, at least one of said first, second and third selectors being provided between said input buffer and latch circuit.

35. The memory device of claim 33 wherein said input circuit inputs said input signal in synchronization with one edge of the clock and said self-test circuit generates said corresponding signal in synchronization with the other edge of said clock.

36. The memory device of claim 33 wherein said self-test activation signal is one or other of a signal supplied from a self-test input terminal or a signal generated in response to a prescribed external command of said memory device, and

in self-test mode, at least some of said selectors are changed over to the external input terminal side in response to a condition of a prescribed external terminal.

37. The memory device of claim 26 wherein a reset signal is supplied to the internal circuitry which includes at least said memory core and memory control circuit, in response to a reset command supplied from a self-test input terminal, and said internal circuit is reset.

38. A memory device comprising:

a memory core having a plurality of memory cells;

a memory control circuit that controls write and read operations to said memory core in response to an external command, in which writing or reading is performed to said memory cells corresponding to an external address;

a self-test circuit that goes into self-test activated condition in response to a self-test activation signal from outside; that generates a test operation command that designates said writing or reading and supplies said command to said memory control circuit, generates a test address and supplies the test address to said memory core, generates test data and supplies the test data as write data to said memory core, and detects defects of said memory device by comparing the read data from said memory core and said test data.

39. The memory device of claim 38 further comprising first and second self-test terminals,

wherein the self-test activation signal is input from said first self-test terminal and a test mode command that designates the test mode is input from said second self-test terminal and, furthermore, said comparison result is output from said second self-test terminal.